



# Low Cost 3.3V Spread Aware Zero Delay Buffer

#### **Features**

- 10 MHz to 100 and 133 MHz Operating Range, compatible with CPU and PCI bus frequencies
- Zero Input-output Propagation Delay
- Multiple Low Skew Outputs
  - □ Output-output skew less than 250 ps
  - □ Device-device skew less than 700 ps
  - □ One input drives five outputs (CY23S05)
  - □ One input drives nine outputs, grouped as 4 + 4 + 1 (CY23S09)
- Less than 200 ps Cycle-to-cycle jitter is compatible with Pentium based systems
- Test mode to bypass PLL (CY23S09 only, see Select Input Decoding for CY23S09 on page 2)
- Available in space saving 16-pin, 150-mil SOIC, 4.4 mm TSSOP, and 150-mil SSOP (CY23S09) or 8-pin, 150-mil SOIC package (CY23S05)
- 3.3V operation, advanced 0.65µ CMOS Technology
- Spread Aware

# **Functional Description**

The CY23S09 is a low cost 3.3V zero delay buffer designed to distribute high speed clocks and is available in a 16-pin SOIC package. The CY23S05 is an 8-pin version of the CY23S09. It accepts one reference input, and drives out five low skew clocks. The -1H versions of each device operate at up to 100 and 133

MHz frequencies and have higher drive than the -1 devices. All parts have on-chip PLLs that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

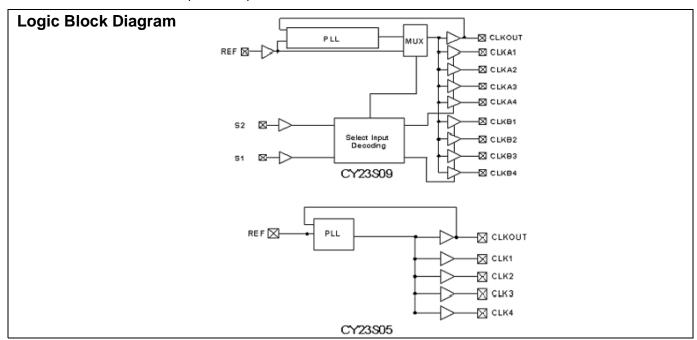
The CY23S09 has two banks of four outputs each, which can be controlled by the select inputs as shown in the Select Input Decoding table on Select Input Decoding for CY23S09 on page 2. If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The CY23S09 and CY23S05 PLLs enter a power down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 12.0  $\mu$ A of current draw (for commercial temperature devices) and 25.0  $\mu$ A (for industrial temperature devices). The CY23S09 PLL shuts down in one additional case, as shown in the Select Input Decoding for CY23S09 on page 2.

Multiple CY23S09 and CY23S05 devices can accept the same input clock and distribute it. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

All outputs have less than 200 ps of cycle-to-cycle jitter. The input to output propagation delay on both devices is guaranteed to be less than 350 ps; the output to output skew is guaranteed to be less than 250 ps.

The CY23S05 and CY23S09 is available in two different configurations, as shown in the Ordering Information on page 6. The CY23S05-1 and CY23S09-1 is the base part. The CY23S05-1H and CY23S09-1H is the high drive version of the -1, and its rise and fall times are much faster than -1.



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## Select Input Decoding for CY23S09

| S2 | S1 | CLOCK A1-A4 | CLOCK B1-B4 | CLKOUT <sup>[1]</sup> | Output Source | PLL Shutdown |
|----|----|-------------|-------------|-----------------------|---------------|--------------|
| 0  | 0  | Three-state | Three-state | Driven                | PLL           | N            |
| 0  | 1  | Driven      | Three-state | Driven                | PLL           | N            |
| 1  | 0  | Driven      | Driven      | Driven                | Reference     | Y            |
| 1  | 1  | Driven      | Driven      | Driven                | PLL           | N            |

### Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve Zero Delay between the input and output. Because the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, to obtain zero input-output delay. If input to output delay adjustments are required, use the above graph to calculate loading differences between the CLKOUT pin and other outputs.

For zero output-output skew, be sure to load all outputs equally. For further information, refer to the application note "CY23S05 and CY23S09 as PCI and SDRAM Buffers."

#### **Spread Aware**

Many systems being designed now use a technology called Spread Spectrum Frequency Timing Generation. Cypress is one of the pioneers of SSFTG development and designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew, which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress application note AN1278, EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs.

#### **Pinouts**

Figure 1. Pin Configuration - CY23S09

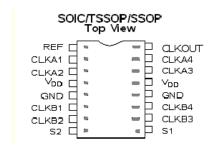
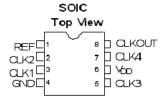


Figure 2. Pin Configuration - CY23S05



Note

<sup>1.</sup> This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.



Table 1. Pin Description for CY23S09

| Pin | Signal                | Description                                    |
|-----|-----------------------|--|
| 1   | REF <sup>[2]</sup>    | Input reference frequency, 5V tolerant input   |
| 2   | CLKA1 <sup>[3]</sup>  | Buffered clock output, bank A                  |
| 3   | CLKA2 <sup>[3]</sup>  | Buffered clock output, bank A                  |
| 4   | $V_{DD}$              | 3.3V supply                                    |
| 5   | GND                   | Ground   |
| 6   | CLKB1 <sup>[3]</sup>  | Buffered clock output, bank B                  |
| 7   | CLKB2 <sup>[3]</sup>  | Buffered clock output, bank B                  |
| 8   | S2 <sup>[4]</sup>     | Select input, bit 2                            |
| 9   | S1 <sup>[4]</sup>     | Select input, bit 1                            |
| 10  | CLKB3 <sup>[3]</sup>  | Buffered clock output, bank B                  |
| 11  | CLKB4 <sup>[3]</sup>  | Buffered clock output, bank B                  |
| 12  | GND                   | Ground   |
| 13  | $V_{DD}$              | 3.3V supply                                    |
| 14  | CLKA3 <sup>[3]</sup>  | Buffered clock output, bank A                  |
| 15  | CLKA4 <sup>[3]</sup>  | Buffered clock output, bank A                  |
| 16  | CLKOUT <sup>[3]</sup> | Buffered output, internal feedback on this pin |

#### Table 2. Pin Description for CY23S05

| Pin | Signal                | Description  |  |
|-----|-----------------------|--|--|
| 1   | REF <sup>[2]</sup>    | Input reference frequency, 5V tolerant input         |  |
| 2   | CLK2 <sup>[3]</sup>   | Buffered clock output                                |  |
| 3   | CLK1 <sup>[3]</sup>   | Buffered clock output                                |  |
| 4   | GND                   | Ground   |  |
| 5   | CLK3 <sup>[3]</sup>   | Buffered clock output                                |  |
| 6   | $V_{DD}$              | 3.3V supply  |  |
| 7   | CLK4 <sup>[3]</sup>   | Buffered clock output                                |  |
| 8   | CLKOUT <sup>[3]</sup> | Buffered clock output, internal feedback on this pin |  |

- Notes

  2. Weak pull down.

  3. Weak pull down on all outputs.

  4. Weak pull up on these inputs.



# **Maximum Ratings**

| Supply Voltage to Ground Potential0.5V to +7.0V             | Maximum Soldering Temperature (10 seconds) 260°C |
|---|--|
| DC Input Voltage (Except REF)0.5V to V <sub>DD</sub> + 0.5V | Junction Temperature                             |
| DC Input Voltage REF0.5V to 7V                              | Static Discharge Voltage                         |
| Storage Temperature65°C to +150°C                           | (per MIL-STD-883, Method 3015)> 2,000V           |

# Operating Conditions for CY23S05SC-XX and CY23S09SC-XX Commercial Temperature Devices<sup>[5]</sup>

| Parameter       | Description                                 | Min | Max | Unit |
|-----------------|---|-----|-----|------|
| $V_{DD}$        | Supply Voltage                              | 3.0 | 3.6 | V    |
| T <sub>A</sub>  | Operating Temperature (Ambient Temperature) | 0   | 70  | °C   |
| C <sub>L</sub>  | Load Capacitance, below 100 MHz             |     | 30  | pF   |
| C <sub>L</sub>  | Load Capacitance, from 100 MHz to 133 MHz   |     | 10  | pF   |
| C <sub>IN</sub> | Input Capacitance                           |     | 7   | pF   |

# Electrical Characteristics for CY23S05SC-XX and CY23S09SC-XX Commercial Temperature Devices

| Parameter                 | Description                        | Test Conditions   | Min | Max   | Unit |
|---------------------------|------------------------------------|---|-----|-------|------|
| $V_{IL}$                  | Input LOW Voltage <sup>[6]</sup>   |   |     | 0.8   | V    |
| V <sub>IH</sub>           | Input HIGH Voltage <sup>[6]</sup>  |   | 2.0 |       | V    |
| I <sub>IL</sub>           | Input LOW Current                  | V <sub>IN</sub> = 0V  |     | 50.0  | μΑ   |
| I <sub>IH</sub>           | Input HIGH Current                 | $V_{IN} = V_{DD}$   |     | 100.0 | μΑ   |
| V <sub>OL</sub>           | Output LOW Voltage <sup>[7]</sup>  | I <sub>OL</sub> = 8 mA (-1)<br>I <sub>OH</sub> = 12 mA (-1H)              |     | 0.4   | V    |
| V <sub>OH</sub>           | Output HIGH Voltage <sup>[7]</sup> | $I_{OH} = -8 \text{ mA } (-1)$<br>$I_{OL} = -12 \text{ mA } (-1\text{H})$ | 2.4 |       | V    |
| I <sub>DD</sub> (PD mode) | Power Down Supply Current          | REF = 0 MHz   |     | 12.0  | μΑ   |
| I <sub>DD</sub>           | Supply Current                     | Unloaded outputs at 66.67 MHz, SEL inputs at V <sub>DD</sub>              |     | 32.0  | mA   |

# Switching Characteristics for CY23S05SC-1 and CY23S09SC-1 Commercial Temperature Devices [8]

| Parameter         | Description   | Test Conditions  | Min      | Тур  | Max           | Unit       |
|-------------------|---|--|----------|------|---------------|------------|
| t1                | Output Frequency  | 30 pF load<br>10 pF load                                     | 10<br>10 |      | 100<br>133.33 | MHz<br>MHz |
|                   | Duty Cycle <sup>[7]</sup> = $t_2 \div t_1$                  | Measured at 1.4V, F <sub>out</sub> = 66.67 MHz               | 40.0     | 50.0 | 60.0          | %          |
| t3                | Rise Time <sup>[7]</sup>                                    | Measured between 0.8V and 2.0V                               |          |      | 2.50          | ns         |
| t <sub>4</sub>    | Fall Time <sup>[7]</sup>                                    | Measured between 0.8V and 2.0V                               |          |      | 2.50          | ns         |
| t <sub>5</sub>    | Output-to-Output Skew <sup>[7]</sup>                        | All outputs equally loaded                                   |          |      | 250           | ps         |
| t <sub>6</sub>    | Delay, REF Rising Edge to CLKOUT Rising Edge <sup>[7]</sup> | Measured at V <sub>DD</sub> /2                               |          | 0    | ±350          | ps         |
| t <sub>7</sub>    | Device-to-Device Skew <sup>[7]</sup>                        | Measured at V <sub>DD</sub> /2 on the CLKOUT pins of devices |          | 0    | 700           | ps         |
| t <sub>J</sub>    | Cycle-to-Cycle Jitter <sup>[7]</sup>                        | Measured at 66.67 MHz, loaded outputs                        |          |      | 200           | ps         |
| t <sub>LOCK</sub> | PLL Lock Time <sup>[7]</sup>                                | Stable power supply, valid clock presented on REF pin        |          |      | 1.0           | ms         |

#### Notes

- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
   REF input has a threshold voltage of V<sub>DD</sub>/2.
   Parameter is guaranteed by design and characterization. Not 100% tested in production.
   All parameters specified with loaded outputs.



# Switching Characteristics for CY23S05SI-1H and CY23S09SI-1H Industrial Temperature Devices<sup>[8]</sup>

| Parameter         | Description   | Test Conditions                                       | Min      | Тур  | Max           | Unit       |
|-------------------|---|---|----------|------|---------------|------------|
| t1                | Output Frequency  | 30 pF load<br>10 pF load                              | 10<br>10 |      | 100<br>133.33 | MHz<br>MHz |
|                   | Duty Cycle <sup>[7]</sup> = $t_2 \div t_1$                  | Measured at 1.4V, F <sub>out</sub> = 66.67 MHz        | 40.0     | 50.0 | 60.0          | %          |
|                   | Duty Cycle <sup>[7]</sup> = $t_2 \div t_1$                  | Measured at 1.4V, F <sub>out</sub> <50.0 MHz          | 45.0     | 50.0 | 55.0          | %          |
| t3                | Rise Time <sup>[7]</sup>                                    | Measured between 0.8V and 2.0V                        |          |      | 1.50          | ns         |
| t <sub>4</sub>    | Fall Time <sup>[7]</sup>                                    | Measured between 0.8V and 2.0V                        |          |      | 1.50          | ns         |
| t <sub>5</sub>    | Output-to-Output Skew <sup>[7]</sup>                        | All outputs equally loaded                            |          |      | 250           | ps         |
| t <sub>6</sub>    | Delay, REF Rising Edge to CLKOUT Rising Edge <sup>[7]</sup> | Measured at V <sub>DD</sub> /2                        |          | 0    | ±350          | ps         |
| t <sub>7</sub>    | Device-to-Device Skew <sup>[7]</sup>                        | Measured at $V_{DD}/2$ on the CLKOUT pins of devices  |          | 0    | 700           | ps         |
| t <sub>8</sub>    | Output Slew Rate <sup>[7]</sup>                             | Measured between 0.8V and 2.0V using Test Circuit #2  | 1        |      |               | V/ns       |
| t <sub>J</sub>    | Cycle-to-Cycle Jitter <sup>[7]</sup>                        | Measured at 66.67 MHz, loaded outputs                 |          |      | 200           | ps         |
| t <sub>LOCK</sub> | PLL Lock Time <sup>[7]</sup>                                | Stable power supply, valid clock presented on REF pin |          |      | 1.0           | ms         |

# **Switching Waveforms**

#### Figure 3. Duty Cycle Timing

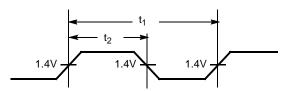


Figure 4. All Outputs Rise/Fall Time

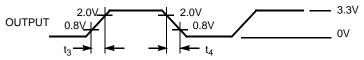


Figure 5. Output-Output Skew

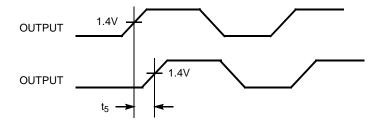
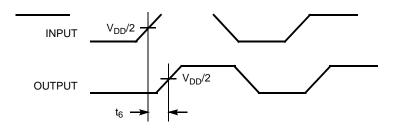


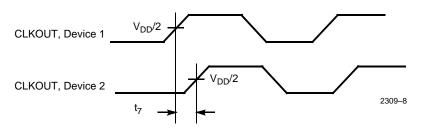
Figure 6. Input-Output Propagation Delay



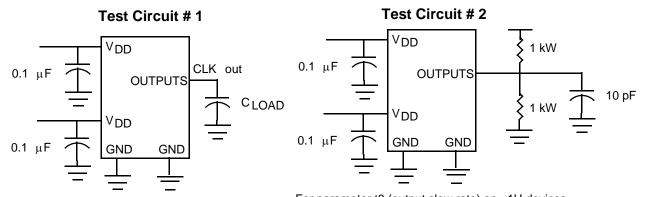


# Switching Waveforms continued

Figure 7. Device-Device Skew



#### **Test Circuits**



# For parameter t8 (output slew rate) on -1H devices

# **Ordering Information**

| Ordering Code               | Package Name | Package Type                        | Operating Range         |
|-----------------------------|--------------|-------------------------------------|-------------------------|
| CY23S05SC-1 <sup>[9]</sup>  | S08          | 8-pin 150-mil SOIC                  | Commercial (0° to 70°C) |
| CY23S05SC-1H <sup>[9]</sup> | S08          | 8-pin 150-mil SOIC                  | Commercial (0° to 70°C) |
| CY23S09SC-1 <sup>[9]</sup>  | S16          | 16-pin 150-mil SOIC                 | Commercial (0° to 70°C) |
| CY23S09SC-1H <sup>[9]</sup> | S16          | 16-pin 150-mil SOIC                 | Commercial (0° to 70°C) |
| CY23S09ZC-1H <sup>[9]</sup> | Z16          | 16-pin 4.4 mm TSSOP                 | Commercial (0° to 70°C) |
| Pb-Free                     |              |                                     |                         |
| CY23S05SXC-1                | SZ08         | 8-pin 150-mil SOIC                  | Commercial (0° to 70°C) |
| CY23S05SXC-1T               | SZ08         | 8-pin 150-mil SOIC – Tape and Reel  | Commercial (0° to 70°C) |
| CY23S05SXC-1H               | SZ08         | 8-pin 150-mil SOIC                  | Commercial (0° to 70°C) |
| CY23S05SXC-1HT              | SZ08         | 8-pin 150-mil SOIC – Tape and Reel  | Commercial (0° to 70°C) |
| CY23S09SXC-1                | SZ16         | 16-pin 150-mil SOIC                 | Commercial (0° to 70°C) |
| CY23S09SXC-1T               | SZ16         | 16-pin 150-mil SOIC – Tape and Reel | Commercial (0° to 70°C) |
| CY23S09SXC-1H               | SZ16         | 16-pin 150-mil SOIC                 | Commercial (0° to 70°C) |
| CY23S09SXC-1HT              | SZ16         | 16-pin 150-mil SOIC – Tape and Reel | Commercial (0° to 70°C) |
| CY23S09ZXC-1H               | ZZ16         | 16-pin 4.4 mm TSSOP                 | Commercial (0° to 70°C) |
| CY23S09ZXC-1HT              | ZZ16         | 16-pin 4.4 mm TSSOP – Tape and Reel | Commercial (0° to 70°C) |

Notes
9. Not recommended for new designs. New designs should use Pb-free devices.



# **Package Diagrams**

Figure 8. 8-Pin (150-Mil) SOIC S08 and SZ08

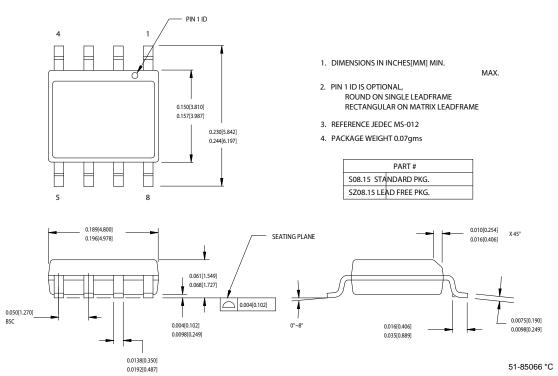
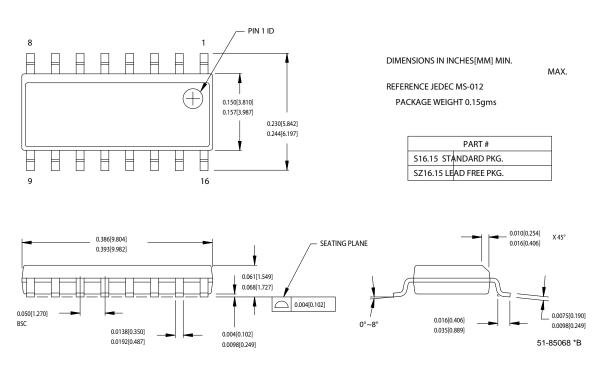


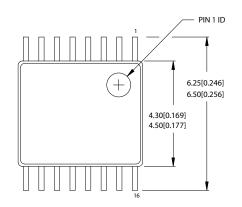
Figure 9. 16-Pin (150-Mil) SOIC S16 and SZ16





# Package Diagrams continued

Figure 10. 16-Pin TSSOP 4.40 mm Body Z16 and ZZ16

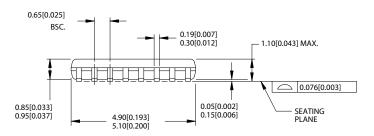


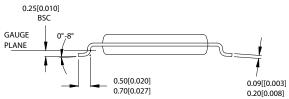
DIMENSIONS IN MM[INCHES] MIN. MAX.

**REFERENCE JEDEC MO-153** 

PACKAGE WEIGHT 0.05 gms

| PART #   |                |  |  |
|----------|----------------|--|--|
| Z16.173  | STANDARD PKG.  |  |  |
| ZZ16.173 | LEAD FREE PKG. |  |  |





51-85091 \*A



### **Document History Page**

| Rev. | ECN No. | Submission<br>Date | Orig. of<br>Change | Description of Change  |
|------|---------|--------------------|--------------------|--|
| **   | 111147  | 11/14/01           | DSG                | Changed from spec number 38-01094 to 38-07296  |
| *A   | 111773  | 02/20/02           | CTK                | Added 150-mil SSOP option  |
| *B   | 122885  | 12/22/02           | RBI                | Added power-up requirements to Operating Conditions  |
| *C   | 267849  | See ECN            | RGL                | Added Lead-Free devices  |
| *D   | 2595524 | 10/23/08           | CXQ/PYRS           | Added device "Status" to Ordering Information  |
| *E   | 2761988 | 09/10/09           | KVM                | Removed obsolete parts from Ordering Information table: CY23S09ZC-CY23S09OC-1, CY23S09OC-1H, CY23S09ZXC-1, CY23S09OXC-1, CY23S09OXC-1H.  Added CY23S05SXC-1T, CY23S05SXC-1HT, CY23S09SXC-1T, CY23S09SXC-1HT, CY23S09ZXC-1HT.  Removed Status column from Ordering Information table; added footnot Updated package names and added numerical temperature range to Ordering Information table.  Removed QSOP package drawing. |

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